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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/512,968	02/24/2000	David R. Hembree	MI22-869	5950

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EXAMINER	
NGUYEN, VINH P	
ART UNIT	**PAPER NUMBER**
2829	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/512,968	HEMBREE, DAVID R.	
	Examiner	Art Unit	
	VINH P NGUYEN	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *64-120* is/are pending in the application.

4a) Of the above claim(s) *66,76,93-96,99 and 100* is/are withdrawn from consideration.

5)☒ Claim(s) *81-92,97,98,101,102,111,117 and 118* is/are allowed.

6)☒ Claim(s) *64-75,77-80,103-110,112-116,119-120* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0604*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 64-65,67,69-75,77-80,103-110,112-115 and 119-120 are rejected under 35 U.S.C. 102(e) as being anticipated by Baker et al (Pat # 4,104,589).

As to claims 64,79 and 108, Baker et al disclose a chuck for testing of semiconductor wafer as shown in figure 1 having a wafer holder (18) having circuitry (11,12,20,22) configured to communicate a process signal from a wafer under test (not shown). It appears that the wafer under test inherently has electrical couplings (electrical contact regions on the bottom surface of the wafer).

It is noted that the limitation of "the wafer holder of the wafer processing apparatus for fabrication of integrated circuitry" as recited in claim 64 and the limitation of "a wafer processing apparatus configured to fabricate integrated circuitry" as recited in claim 108 are intended uses and they are not given any patentable weights. Furthermore, it is noted that the word "process" recited in claim 79 is defined as a series of actions, changes, or functions bringing about a result, testing environment would be qualified for this definition. However the term "process" is not necessary related to a method of making.

As to claim 65, Baker et al teach that the electrical coupling /circuitry (11,12,20,22) are connected to a measuring sensing means (read as "data gathering device") (see column 2, lines 45-68).

As to claim 67, it appears that the electrical coupling /circuitry (11,12,20,22) are qualified as "the interconnect configured to electrically couple the first surface and the second surface of the wafer holder (18)

As to claims 69,77, Baker et al teach that there are a plurality of electrical couplings (11,12,20,22) coupled with a plurality of electrical couplings (electrical contact regions) on the bottom surface of the wafer.

As to claim 70, Baker et al disclose a chuck (18).

As to claim 71, the chuck (18) of Baker et al is configured to receive a production wafer (wafer under test) .

As to claims 72, 74, Baker et al teach that the wafer holder includes vacuum chambers (28) for receiving a vacuum to couple the production wafer/wafer under test with the chuck (18) (see column 3, lines 1-8).

As to claim 73, the wafer holder of Baker includes intermediate members (11,12) adapted to couple with the chuck (18)

As to claim 75, Baker et al teach that the wafer holder (18) includes a conductive column (11,12) extending outward from first and second surfaces of the wafer holder (18).

As to claims 78 and 80, Baker et al teach that wafer holder (18) is adapted to expose the wafer to a processing environment to process the wafer. It is noted that the word "process"

recited in claim 78 is defined as a series of actions, changes, or functions bringing about a result, testing environment would be qualified for this definition. However the term "process" is not necessary related to a method of making.

As to claim 103, the wafer holder of Baker et al is configured to support a wafer under test for processing within the processing apparatus. It is noted that the limitation of "to form a plurality of discrete integrated circuits of a plurality of respective dies to be singulated from the wafer at a subsequent moment in time" is considered as intended use and this limitation is not given any patentable weight.

As to claim 104, the wafer holder of Baker et al is configured to expose a wafer under test to a processing environment (testing environment) within the wafer processing apparatus. It is noted that the limitation of "to form a plurality of discrete integrated circuits of a plurality of respective dies to be singulated from the wafer at a subsequent moment in time" is considered as intended use and this limitation is not given any patentable weight.

As to claim 105, the device of Baker et al also includes a processing area of wafer processing apparatus configured to process a wafer supported using the wafer holder (18). It is noted that the limitation of "to fabricate a plurality of discrete integrated circuits of a plurality of respective dies to be singulated from the wafer at a subsequent moment in time" is considered as intended use and this limitation is not given any patentable weight.

As to claim 106, the processing apparatus of Baker et al is configured to process a wafer under test supported using the wafer holder. It is noted that the limitation of "to fabricate a plurality of discrete integrated circuits of a plurality of respective dies to be singulated from the wafer at a subsequent moment in time" is considered as intended use and this limitation is not given any patentable weight.

As to claim 107, it appears that the wafer of Baker et al includes a plurality of integrated circuit dies prior to singulation of at least one of the die at a subsequent moment in time.

As to claims 109, 116, the process signal of Berger et al is an electrical signal using an electrical coupling (26) of the wafer holder (16) in electrical contact with an electrical coupling (electrical contact regions) on the bottom surface of the wafer.

As to claims 110, the communicated signals includes information regarding processing of the wafer. It is noted that word "process" recited in claim 110 is defined as a series of actions, changes, or functions bringing about a result, testing environment would be qualified for this definition. However the term "process" is not necessary related to a method of making.

As to claim 112, it appears that the electrical coupling (11,12) of the wafer holder (18) is electrically conductive to establish an electrical connection with the electrical coupling of the wafer where electrons of the signals are exchanged between the electrical couplings of the wafer holder (18) and the wafer .

As to claim 113, it appears that the signals from the wafer is generated by its electrical circuitry (electrical contact regions on the bottom surface of the wafer).

As to claims 114, the signals of Baker et al are electrical signals.

As to claims 115, the process signals of Baker et al include information regarding processing of the wafer. It is noted that the limitation of "for fabrication of integrated circuitry using the wafer processing apparatus" is considered as intended use, therefore this limitation is not given any patentable weight.

As to claims 119, the communicated signals of Baker et al include information regarding processing of the wafer. It is noted that the limitation of "for fabrication of integrated circuitry using the wafer processing apparatus" is considered as intended use, therefore this limitation is not given any patentable weight.

As to claim 120, Baker et al teach that electrical couplings of the wafer and the wafer holder are in electrical contact with one another to communicate the signals comprising electrical signals between the at least one wafer and the wafer holder (18).

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 64-65,67-71,75,77-80,103-110,112-115 and 119-120 are rejected under 35 U.S.C. 102(e) as being anticipated by Berger et al (Pat # 6,020,750).

As to claims 64,79 and 108, Berger et al disclose a wafer test and burn-in platform as shown in figure 2 having a wafer holder (16) having circuitry (26,28) configured to communicate a process signal from a received wafer (12) having electrical couplings (electrical contact regions on the bottom surface of the wafer).

It is noted that the limitation of "the wafer holder of the wafer processing apparatus for fabrication of integrated circuitry" as recited in claim 64 and the limitation of "a wafer processing apparatus configured to fabricate integrated circuitry" as recited in claim 108 are intended uses and they are not given any patentable weights. Furthermore, it is noted that the word "process" recited in claim 79 is defined as a series of actions, changes, or functions bringing about a result, testing environment would be qualified for this definition. However the term "process" is not necessary related to a method of making.

As to claim 65, Berger et al teach that the electrical coupling /circuitry (26,28) on the connector contact surface (20) are connected to a contactor system (read as "data gathering device").

As to claim 67, it appears that the upper contact (26) and lower contact (28) are qualified as "the interconnect configured to electrically couple the first surface and the second surface of the wafer holder.

As to claim 68, Berger et al teach that the first/top surface of the wafer holder (16) is configured to face a receiver wafer (wafer under test) "12" and the second surface is configured to face a chuck (14).

As to claims 69,77, Berger et al teach that there are a plurality of electrical couplings (26) coupled with a plurality of electrical couplings (electrical contact regions) on the bottom surface of the wafer.

As to claim 70, Berger et al disclose a chuck (14).

As to claim 71, the chuck (140 of Berger et al is configured to receive a production wafer (wafer under test) "22".

As to claim 75, Berger et al teach that the wafer holder (16,26,28) includes a conductive column (26,28) extending outward from first and second surfaces of the wafer holder (16).

As to claims 78 and 80, Berger et al teach that wafer holder (16) is adapted to expose the wafer (22) to a processing environment to process the wafer. It is noted that the word "process" recited in claim 78 is defined as a series of actions, changes, or functions bringing about a result, testing environment would be qualified for this definition. However the term "process" is not necessary related to a method of making.

As to claim 103, the wafer holder of Berger et al is configured to support a wafer under test for processing within the processing apparatus. It is noted that the limitation of "to form a

plurality of discrete integrated circuits of a plurality of respective dies to be singulated from the wafer at a subsequent moment in time" is considered as intended use and this limitation is not given any patentable weight.

As to claim 104, the wafer holder of Berger et al is configured to expose a wafer under test to a processing environment (testing environment) within the wafer processing apparatus. It is noted that the limitation of "to form a plurality of discrete integrated circuits of a plurality of respective dies to be singulated from the wafer at a subsequent moment in time" is considered as intended use and this limitation is not given any patentable weight.

As to claim 105, the device of Berger et al also includes a processing area of wafer processing apparatus configured to process a wafer supported using the wafer holder (18). It is noted that the limitation of "to fabricate a plurality of discrete integrated circuits of a plurality of respective dies to be singulated from the wafer at a subsequent moment in time" is considered as intended use and this limitation is not given any patentable weight.

As to claim 106, the processing apparatus of Baker et al is configured to process a wafer under test supported using the wafer holder. It is noted that the limitation of "to fabricate a plurality of discrete integrated circuits of a plurality of respective dies to be singulated from the wafer at a subsequent moment in time" is considered as intended use and this limitation is not

given any patentable weight.

As to claim 107, it appears that the wafer of Baker et al inherently includes a plurality of integrated circuit dies prior to singulation of at least one of the die at a subsequent moment in time.

As to claims 109, 116, the process signal of Berger et al is an electrical signal using an electrical coupling (26) of the wafer holder (16) in electrical contact with an electrical coupling (electrical contact regions) on the bottom surface of the wafer.

As to claims 110, the communicated signals includes information regarding processing of the wafer. It is noted that word "process" recited in claim 110 is defined as a series of actions, changes, or functions bringing about a result, testing environment would be qualified for this definition. However the term "process" is not necessary related to a method of making.

As to claim 112, it appears that the electrical coupling (26,28) of the wafer holder (16) is electrically conductive to establish an electrical connection with the electrical coupling of the wafer where electrons of the signals are exchanged between the electrical couplings of the wafer holder and the wafer (22).

As to claim 113, it appears that the signals from the wafer (22) is generated by its electrical circuitry (electrical contact regions on the bottom surface of the wafer).

As to claims 114, the signals of Berger et al are electrical signals.

As to claims 115, the process signals of Berger et al include information regarding processing of the wafer. It is noted that the limitation of "for fabrication of integrated circuitry using the wafer processing apparatus" is considered as intended use, therefore this limitation is not given any patentable weight.

As to claims 119, the communicated signals of Berger et al include information regarding processing of the wafer. It is noted that the limitation of "for fabrication of integrated circuitry using the wafer processing apparatus" is considered as intended use, therefore this limitation is not given any patentable weight.

As to claim 120, Berger et al teach that electrical couplings of the wafer and the wafer holder are in electrical contact with one another to communicate the signals comprising electrical signals between the at least one wafer (22) and the wafer holder (16).

5. Claims 81-92,97-98,101-102,111,117-118 are allowable since the prior art does not disclose an electronic device workpiece processing apparatus having an electronic workpiece including a sensor and an electrical coupling configured to provide electrical connection of the sensor with the electrical coupling of the second surface of the intermediate member.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VINH P NGUYEN whose telephone number is (571)-272-1964. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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ART UNIT 2829
09/03/04